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HIGH LIFETIME GA-DOPED CZ-SI FOR CARRIER SELECTIVE JUNCTION SOLAR CELLS

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ABSTRACT: Industrial mass production of solar cells is moving towards carrier selective junction solar cells with passivating contacts such as TOPCon, POLO and HJT solar cells. At the same time many manufacturers consider switching from p-type Cz-Si to n-type Cz-Si wafers.
This contribution indicates that Ga-doped p-type Cz-Si material is still a viable option for the new type of devices while giving an opportunity to benefit from 8-10% lower wafer cost. In that respect a Ga-doped Cz-Si ingot has been specified and characterized. We report minority carrier diffusion lengths that are an order of magnitude larger than the thickness of the studied HJT and TOPCoRE devices. So far best p-type HJT solar cells perform 0.2 % absolute lower in efficiency than co-processed n-type reference HJT solar cells. Best TOPCoRE solar cells on Ga doped Cz-Si, however, show a 0.2% to 0.3% higher efficiency than their co-processed n-type TOPCon counterparts.
Keywords: Ga-doped Cz-Si, carrier selective junctions, minority carrier lifetime, light induced improvement

1 INTRODUCTION

For decades, p-type crystalline silicon wafers with resistivities of 0.5-3.0 Ω·cm have been the work horse in mass production of Al BSF and PERx-type solar cells. As the performance of such solar cells improved and diamond wire sawing of wafers enabled a reduction of wafering cost there was a clear shift from multicrystalline to Czochralski silicon (Cz-Si) monocrystalline wafers [1]. Now with a next transition to passivated contact device architectures such as tunnel oxide passivated contact (TOPCon), poly silicon on oxide (POLO) and heterojunction technology (HJT) many PV manufacturers prepare for switching to n-type Cz-Si. Outstanding solar cell efficiencies have been reported on such material [2-5].

However, moving from p-type to n-type Cz-Si comes at an additional cost for the wafer material. During the last years the cost as tracked for instance at PVInsights [6] for n-type compared to p-type Cz-Si wafers has been 8-10% higher. Leading wafer manufacturers see fundamental reasons why n-type Cz-Si wafers will remain more expensive than their p-type counterparts. This contribution indicates that switching the doping level towards higher resistivities and the doping species to Ga doping offers an alternative that might be economically advantageous compared to n-type material.

A complete Ga-doped Cz-Si ingot has been grown according to our specification. The base resistivity is in the range 5-12 Ω·cm after thermal donor annihilation. We investigate tunnel oxide passivated contact rear emitter (TOPCoRE) [7] and heterojunction technology (HJT) solar cells [8] and respective precursors for lifetime and implied open circuit voltage (i-V_{OC}) assessment. For this purpose, wafers are representatively selected along the ingot length. Thus, we look at material aspects with respect to high as well as to low temperature processing.

We demonstrate that such material allows for minority carrier diffusion lengths that are an order of magnitude larger than the solar cell thickness. Those diffusion lengths are larger than those typically obtained for 1 Ω·cm n-type Cz-Si material and should not limit the performance of the discussed solar cells.

Furthermore, we look at stability aspects of such devices with respect to typical conditions such as illumination at room and elevated temperatures as encountered in PV modules in the field. Those investigations are reported in a parallel publication [9]. Surprisingly, we observe a significant light or injection induced improvement in minority carrier lifetime (MCL), i-V_{OC}, V_{OC}, pseudo fill factor (pFF) and FF and a moderate improvement in short circuit current density (J_{SC}) within a very short illumination time (second to minute range) that is leading to efficiency improvement of up to 0.8% absolute on TOPCoRE solar cells. This improvement is clearly higher than improvement observed in parallel for TOPCon devices on 1 Ω·cm n-type Cz-Si that have been co-processed. The rear junction p-type Cz-Si TOPCoRE and front junction n-type Cz-Si TOPCon solar cells apply in this comparison the same processing sequence prior to studying the stability under illumination. The best TOPCoRE solar cells on p-type Cz-Si perform 0.2% absolute better in efficiency than co-processed TOPCon reference solar cells.

For the HJT low temperature processing route the same processing sequence has been applied as well to, both, 5-12 Ω·cm Ga-doped p-type and to 1 Ω·cm n-type Cz-Si wafers. In this case we compare front junction p-type Cz-Si solar cells to n-type Cz-Si rear junction solar cells. So far, we see a gap in average efficiency of 0.36 % in favor of the n-type reference process for which the processing sequence has been developed. The lower HJT performance on the p-type wafers suffers so far from a lower FF while J_{SC} and V_{OC} are slightly higher compared to the n-type reference HJT solar cells. It is not clear yet whether this gap is fundamental or can be solved by adapted processing. However, it can be stated that the material quality (diffusion length) of the high resistivity Ga-doped p-type Cz-Si is not limiting the p-type HJT cell performance. A high temperature pre-treatment step to de-activate thermal donors and to getter potential transition metal impurities does not seem to be required to obtain good solar cell performance along the complete ingot even though a small i-V_{OC} improvement from gettering is noticed. The advantage in i-V_{OC}, MCL and V_{OC} for gettered samples increases with increasing ingot length.

2 LOW TEMPERATURE PROCESSING

The heterojunction technology (HJT) offers a low

temperature processing route. In all processing steps, wafer temperatures do not exceed 250 °C. Cz-Si material contains oxygen related thermal donors (TDs) in the as received state [10]. For moderately doped material such as the investigated high resistivity Ga-doped p-type Cz-Si material the base resistivity is significantly increased by those TDs if no thermal processing at elevated temperatures is applied to de-activate the thermal donors. Material improvement from processing steps like external impurity gettering during diffusion processes may not be applied during HJT processing. For a part of the studied i-V_{OC} precursors and solar cells we apply prior to HJT processing a $POCl_3$ gettering step followed by a complete removal of the diffused and gettered zone by wet chemical etching. This pre-gettering step does not only getter impurities but also annihilates TDs. With that comparative investigation we intend to quantify potential improvement that could be expected by adding such additional processing steps.

2.1 Ingot material evaluation

For both, high and low temperature routes, wafers have been selected in equidistant steps along the complete ingot length of 10000 wafers from seed to tail end of the Ga doped Cz-Si ingot. Figure 1 shows the processing sequence for the low temperature HJT route including $POCl_3$ gettering prior to HJT processing for half of the selected wafers.

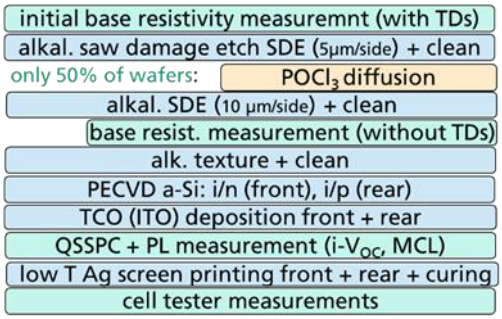

Figure 1: Evaluation process sequence for HJT precursors and solar cells

The high temperature diffusion step for the pre-gettered wafers is sufficient to completely de-activate oxygen related thermal donors in the material. As the etching steps are the same for gettered and non-gettered wafers and as the etching completely removes the diffused region (10 µm per side) the resistivity with and without thermal donors may be compared. Figure 2 shows this comparison along the complete ingot length. A significant difference is visible in the seed near region of the Ga-doped Cz-Si ingot. In this region there are the highest oxygen concentrations along the ingot.

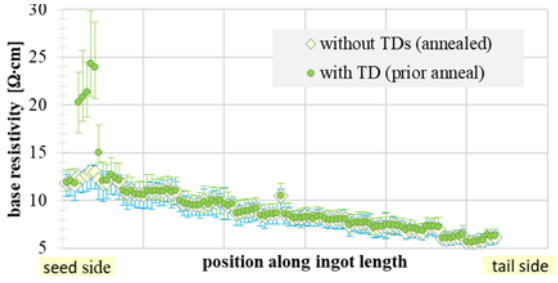

Figure 2: Base resistivity measurement results along the complete Ga doped Cz-Si ingot for wafers with and without TDs.

The oxygen-related thermal donor concentration in the seed near region compensates to a large extent the p-type Ga doping concentration in this region. After high temperature processing, however, the thermal donors are de-activated and the resistivity along the ingot follows the typical resistivity gradient caused by segregation behavior of the Ga doping atoms at the melt/solid interface during ingot growth. The Ga doping concentration increases from seed to tail end of the ingot.

Figure 3 shows the effective minority carrier lifetime (MCL) as assessed at an injection level of $5*10^{15}$ cm^{-3} for the asymmetric solar cell precursors that had been representatively selected along the complete ingot length. This assessment is performed after TCO deposition (see Figure 1). The base resistivity shown in green (right y axis) indicates the position of the precursors in the ingot.

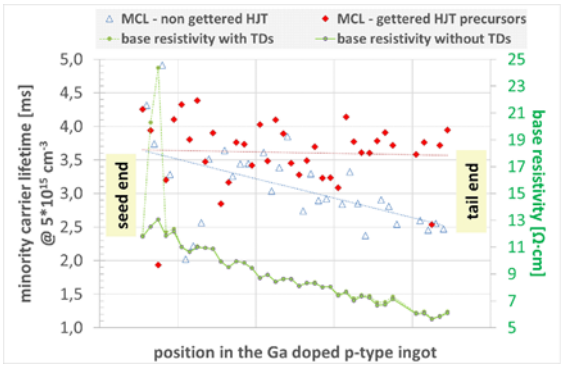

Figure 3: Evaluation of effective minority carrier lifetime along the Ga-doped ingot for HJT i-Voc precursors with and without pr-gettering prior to HJT processing.

The pre-gettering step that had been performed for half of the precursors improved the effective MCL compared to HJT precursors that have not seen any high temperature processing step. This improvement in effective MCL increases towards the tail end of the ingot where more getterable impurities (transition metals) can be expected due to segregation during ingot growth. However, with an effective MCL of more than 2.5 ms along the complete p-type ingot it is unlikely that the minority carrier diffusion length is limiting the solar cell performance. Due to the 2.6 times higher mobility of electrons (minority carrier in p-type Si) compared to holes (minority carrier in n-type Si) the diffusion length is clearly higher than for our reference process on 1 Ω·cm n-type Cz-Si and in all cases more than 10 times of the solar cell thickness. From that perspective the chosen Ga doped Cz-Si material is consequently not limiting the solar cell performance.

2.2 HJT solar cell results

Applying the processing sequence described in section 2.1 (see Figure 1) HJT solar cells have been co-processed on n-type reference Cz-Si wafers (1 Ω·cm) and those selected from the p-type Ga-doped Cz-Si ingot. The processing sequence has been applied as optimized for n-type Cz-Si. Thus, for the Ga-doped wafers the p-n junction is on the front side while for the n-type material it remains on the rear. Neither a-Si layers nor TCO have been adapted yet for the Ga-doped Cz-Si wafers. The resulting solar cell efficiency along the Ga-doped Cz-Si ingot is in average 0.36% absolute lower than for the reference process on n-

type Cz-Si. The delta efficiency distribution is shown in Figure 4.

The HJT solar cells on high resistivity Ga-doped p-type Cz-Si show in average a 0.3 mA/cm^2 higher J_{SC}. This is likely a consequence from having the junction at the front. For the pre-gettered wafers the V_{OC} is in average 2.5 mV higher than for the n-type HJT solar cells. On the non-gettered p-type wafers V_{OC} on resulting HJT solar cells is in the same range as for (non-gettered) n-type wafers. The performance difference is so far dominated by a significantly (+1.5% absolute in average) higher fill factor for the n-type material. There is no significant difference in efficiency between pre-gettered and non-gettered p-type Cz-Si HJT solar cells. Neither do we see a change in performance for non-gettered p-type HJT solar cells in the region of the ingot that has significantly higher base resistivity due to the presence of thermal donors. The scattering in FF so far dominates the efficiency distribution.

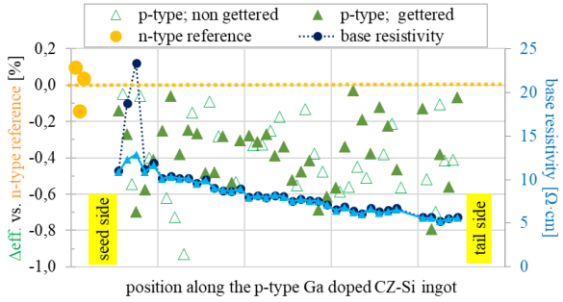

Figure 4: delta efficiency distribution along the Ga doped p-type ingot compared to the n-type reference case

The efficiency disadvantage (-0.36% absolute) results at this stage of evaluation (not yet optimized) for the Ga doped p-type ingot in a cost of ownership [11] penalty that is slightly higher than the cost advantage from the 8-10% lower p-type Cz-Si wafer prices. The top efficiencies in this first evaluation differ only by 0.2% absolute in favor of the n-type reference. Therefore, HJT process optimization for p-type wafers leading to higher FF values will be required to benefit from an economical advantage when using this alternative wafer source. Such improvement seems possible when adapting the processing sequence. In addition, there is still room for going to a slightly lower resistivity range.

3 HIGH TEMPERATURE PROCESSING

High temperature processing routes for carrier selective junction solar cells such as TOPCon are considered to have economic advantages [11] compared to HJT with respect to levelized cost of energy (LCOE) and capital expenditure (CAPEX). The TOPCoRE (on p-type Cz-Si) or TOPCon solar cells (on n-type Cz-Si) apply high-temperature processing steps including boron diffusion, doped poly-silicon deposition, annealing as well as metallization firing. Therefore, Cz-Si material should preferably be compatible with these high-temperature processing steps that might alter the material quality.

3.1 Precursors with symmetric TOPCon passivation

To assess the effective MCL that can be achieved when applying a $POCl_3$ pre-gettering step and TOPCoRE passivation on both, front and rear flat surfaces, we applied the processing sequence depicted in Figure 5 to wafers that had been selected at equidistant locations along the complete Ga-doped ingot length. In that way, both, the response of the material along the complete ingot of 10000 wafers to high T processing including gettering as well as the surface passivation by the TOPCoRE passivation stack can be assessed. Results are shown in Figure 6. Those effective minority carrier lifetimes of the Ga-doped Cz-Si correspond at all sections of the ingot to diffusion lengths that are at least an order of magnitude larger than the device thickness and should not limit the solar cell performance. This is a requirement for a rear junction high efficiency solar cell. Furthermore, excellent TOPCoRE passivation is demonstrated with effective median MCL values exceeding 4 ms along the complete ingot without a clear MCL trend along the ingot.

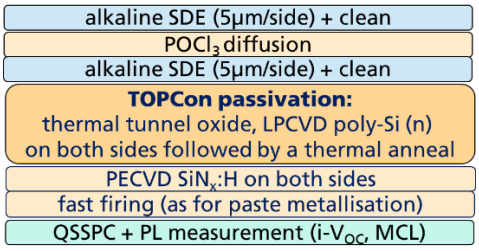

Figure 5: Process sequence for symmetric TOPCoRE effective MCL precursors with flat surfaces.

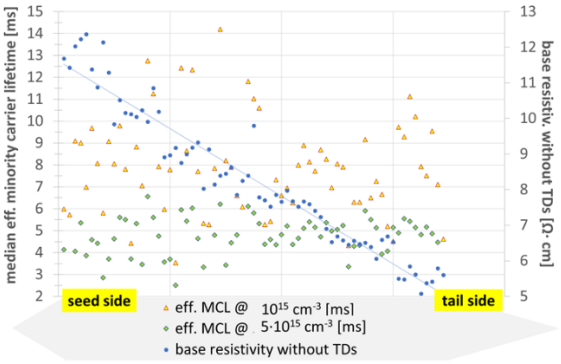

Figure 6: Median effective MCL at two injection levels for TOPCoRE passivation on wafers selected along the Ga-doped Cz-Si ingot.

3.2 TOPCoRE versus TOPCon solar cells

The processing sequence depicted in Figure 7 applied to both, n-type and p-type Cz-si wafers results in TOPCon front junction [12] and TOPCoRE rear junction solar cells, respectively.

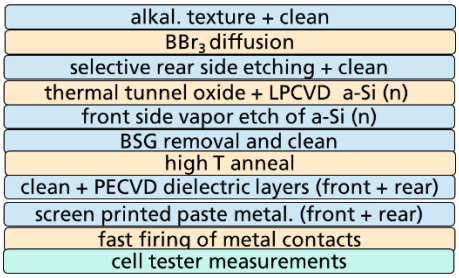

Figure 7: Process sequence for TOPCon (n-type Cz-Si) front junction and TOPCoRE (p-type Cz-Si) rear junction solar cells.

The processing sequence had been originally optimized for n-type wafers of 1 Ω·cm resistivity. Nevertheless, already a first comparison identified that similar solar cell performance can be achieved. Unfortunately, for the delta efficiency evaluation (co-processed n-type TOPCon cells serving as reference) shown in Figure 8 we noticed unwanted variation in one processing step, namely the single sided gas phase etching of poly-Si(n) that had been deposited on top of the front BSG layer and the wafer edges.

The TOPCoRE solar cells encircled in green towards the tail end of the ingot performed better than the reference TOPCon process. All these cells had been co-processed in vapor etching in one batch while other TOPCoRE cells of neighboring regions in the ingot and from the first half of the ingot had been processed in other vapor etching batches. Therefore, the scattering in efficiency along the ingot is not dominated by material properties but by processing during single sided vapor etch. However, this indicated to us a road how TOPCoRE processing can result in advantageous solar cell performance as compared to TOPCon processing.

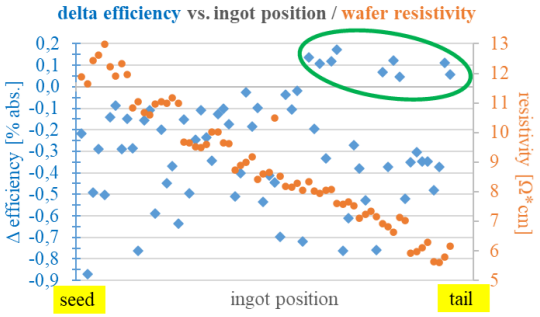

Figure 8: Delta efficiency distribution of TOPCoRE solar cells from Ga doped p-type wafers that been selected along the complete Cz-Si ingot. The efficiency is compared to the TOPCon reference process on n-type Cz-Si.

Furthermore, we identified to our surprise that for our processing sequence (identical processing steps for TOPCon and TOPCoRE), that finished solar cells show a very rapid light induced improvement (LII) behavior. Within repeated cell tester flashes (80 ms, 1 sun) there is a very significant improvement in efficiency within an accumulated (1 sun) illumination duration in the order of seconds to a few minutes. The improvement is more pronounced for TOPCoRE than for TOPCon solar cells that have been co-processed and leads to an improvement of upto 0.8% absolute in efficiency. That LII behavior results from MCL improvement, i-V_{OC} and V_{OC} improvement, pFF and FF improvement, and in case of TOPCoRE solar cells also from J_{SC} and series resistance improvement. More details on that finding are given in the accompanying journal publication to this conference contribution [9]. The observed LII is annoying for cell tester characterization but would not have negative impact on module performance in the field due to the very fast improvement as compared to a comparably slow relaxation to the original state when stored in the dark. Investigations to understand the cause(s) of this LII are on-going. In parallel also investigations with respect to LeTID behavior are ongoing and reported in [9].

Besides the significant improvement from LII, we applied an additional processing step to further improve the efficiency of TOPCoRE and TOPCon solar cells. After contact firing Laser Enhanced Contact Optimization (LECO) [13] has been applied to further increase the FF of our solar cells. With adapted LECO processing for both, TOPCoRE and TOPCon solar cells, we see by now for co-processed solar cells an advantage of 0.2% to 0.3% absolute in efficiency for TOPCoRE solar cells on the studied Ga-doped p-type Cz-Si material as compared to TOPCon on n-type Cz-Si of 1 Ω·cm resistivity. That finding needs to be confirmed with more statistics and on wafers selected from all regions of the ingot in future.

4 CONCLUSIONS

We specified, ordered and analyzed a p-type Ga-doped Cz-Si ingot with a comparably high resistivity range and compared it to n-type material that is typically used for HJT and TOPCon solar cells.

The p-type Cz-Si material has not only a significant cost advantage compared to commercially available n-type material but showed also along the complete ingot minority carrier diffusion lengths that do not limit the solar cell efficiency of carrier selective junction and passivated contact solar cells, such as HJT and TOPCoRE. The diffusion length for the studied Ga doped p-type material is even superior to that of the n-type reference Cz-Si material.

Both, high temperature and low temperature processing routes have been applied to manufacture i-V_{OC} and MCL precursors as well as industrially relevant high efficiency solar cells. In both cases, HJT processing and TOPCoRE processing the processing sequence was kept identical as for the reference process on n-type Cz-Si. By this the p-n junction moved for HJT from rear to front and for TOPCon/TOPCoRE from front to rear.

HJT precursors just prior to metallization show i-V_{OC} values above 745 mV [9] and MCL above 2.5 ms along the complete studied p-type ingot. If pre-gettering is applied prior to HJT processing the i-V_{OC} and MCL is slightly improved. Towards the tail end of the ingot improvement from pre-gettering is more pronounced. So far, the outstanding diffusion length and i-V_{OC} values >750 mV result in improved J_{SC} and in case of pre-gettered HJT cells also in higher V_{OC} values for p-type compared to n-type HJT solar cells. Unfortunately, the FF of the p-type Cz-Si HJT solar cells is inferior to the counterparts on n-type Cz-Si and suffers from large scattering in FF. Thus, in average the resulting efficiency is so far 0.36% lower for the p-type material. Respective best efficiencies of co-processed p-type HJT solar cells are 0.2% lower than for the n-type reference process. For HJT a FF improvement will be required to make p-type Cz-Si due to its lower wafer cost commercially advantageous.

For TOPCoRE application in high temperature processing the material proved also to result in excellent effective MCL when evaluated with symmetric lifetime samples. The minority carrier diffusion length showed to be along the complete ingot at least an order of magnitude higher than the device thickness of TOPCoRE solar cells.

In addition, we could demonstrate that the rear junction TOPCoRE solar cells have not only for lab cells [7] but also for industrial application the potential to result in better solar cell performance than their n-type counterparts. Thus, there are two commercial advantages, one coming from the significantly lower wafer cost and one from the better solar cell performance that make this route highly attractive. With the currently high wafer prices and the price difference between p-type and n-type

Cz-Si wafers those advantages for p-type TOPCoRe solar cells offer in a 10 GW/year TOPCon production scenario the potential to save > 100 million US$/year.

With respect to long term stability of the respective material we do not see disadvantages for the studied Ga doped p-type Cz-Si compared to n-type Cz-Si. To our surprise we see in both cases a light induced improvement LII behavior on a very short time scale that seems more pronounced for the back junction TOPCoRE solar cells. The cause of this LII is not yet fully understood and further under investigation. We do not find this behavior on low temperature processed HJT solar cells nor on the TOPCoRE lifetime precursors. With respect to LeTID we need to extend our investigations from lifetime samples to solar cells. So far, we do not see a disadvantage for the Ga-doped p-type compared to n-type Cz-Si.

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